[*FLIP-CHIP PACKAGE SUBSTRATE*]

Abstract of Disclosure

A flip-chip package substrate comprising a plurality of wiring layers, at least one insulation layers and at least one conductive plugs. The wiring layers are sequentially stacked such that an insulation layer is always sandwiched between two neighboring wiring layers. The conductive plug passes through the insulation layer for connecting with wiring layers. The uppermost wiring layer has a plurality of bump pads while the bottommost wiring layer has a plurality of ball pads. The bump pads on the uppermost wiring layer are organized into bump pad rings. Similarly, the ball pads on the bottommost wiring layer are organized into ball pad rings. Relative position of both the bump pad rings and the ball pad rings are organized according to functions in sequential order so that the wiring distance from the bump pads down to the ball pads is optimized.

Figures